

# An Explicit Construction of Euler Circuits in Shuffle Nets and Related Networks

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In this paper, we present a construction of Euler circuits for some circular multistage interconnection networks, which have a uniform structure between consecutive stages.

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## 1. INTRODUCTION

Shuffle nets have been introduced for lightwave communications networks [1]. The shuffle net (SN) of order  $n$  as defined in [1] is a circular Omega network [7] and has  $n2^n$  vertices organized in  $n$  stages of  $2^n$  vertices each. For connectivity purposes, it is of interest to designate Euler circuits in these and associated networks that are used for the purpose of parallel processing and communication.

A simple construction is based on *bar-threading* in the vertices of all but one of the columns of the SN and either bar-threading or *cross-threading* in a selected column. Bar-threading and cross-threading are defined exactly in the next section. We propose a procedure to designate one possible set of vertices to be cross-threaded. The procedure is suitable for SNs as well as for the following variants:

- (1)  $k$ -stage circular shuffle exchange networks with  $2^n$  vertices per stage.
- (2)  $k$ -stage circular uniform minimal full-access (UMFA) networks.
- (3)  $k$ -stage circular  $m$ -ary perfect shuffle networks with  $m^n$  vertices per stage.

In all these variants, the structure of the graph between any two consecutive stages is identical.

## 2. CONSTRUCTION OF EULERIAN CIRCUITS

The SN is a directed graph with  $n$  stages, each one having  $2^n$  vertices. In each stage, we label the  $2^n$  vertices by all the binary  $n$ -tuples. Vertex  $(x_1, x_2, \dots, x_n)$  in stage  $i$ ,  $0 \leq i \leq n - 1$ , has two *directed edges*, one to vertex  $(x_2, \dots, x_n, 0)$  and a second to vertex  $(x_2, \dots, x_n, 1)$ . Each vertex  $(x_1, x_2, \dots, x_n)$  has two *points* arranged vertically, the upper is labeled by  $(x_1, x_2, \dots, x_n, 0)$  and the lower is labeled by  $(x_1, x_2, \dots, x_n, 1)$ . We say that vertex  $(x_1, x_2, \dots, x_n)$  is *bar-threaded* if the edge from point  $(x_1, x_2, \dots, x_n, x_{n+1})$  is to point  $(x_2, \dots, x_n, x_{n+1}, x_1)$  in the next stage and that it is *cross-threaded* if the edge from point  $(x_1, x_2, \dots, x_n, x_{n+1})$  is to point  $(x_2, \dots, x_n, x_{n+1}, \bar{x}_1)$  in the next stage. The network is circular, i.e., stage  $n - 1$  is followed by stage 0.

A construction of an Eulerian circuit in the SN is very similar to the construction of de Bruijn sequences [4]. For this construction, we need the following definitions: The *weight*  $W(X)$  of a point  $X$  is the number of ONES in  $X = (x_1, x_2, \dots, x_n, x_{n+1})$ . Let all the vertices be bar-threaded. Then, starting at any point  $X$  and going along the edges, we travel along a circuit whose points have the same weight since the representation of any point  $Y$  along this circuit is a cyclic shift of  $X$ . Each such circuit is called a *primitive circuit*. The *weight*  $W(C)$  of a primitive circuit  $C$  is defined to be equal to the weight of each of its points. A *crossed SN* is an SN with some vertices cross-threaded and the rest bar-threaded. If all the vertices are bar-threaded, the SN is said to be *all-bars*. We formulate the following observation in terms of

**Lemma 2.1.** Given a crossed SN, then changing the threading of a vertex from bar to cross or from cross to bar results in either the joining of two circuits into one or the breaking one circuit into two.

It follows that to form an Eulerian circuit one can start from an all-bars SN, proceed to identify its primitive circuits, and, finally, join them by cross-threading  $T - 1$  appropriate vertices, where  $T$  is the number of primitive circuits. To calculate  $T$ , we first note the following property of the primitive circuits:

**Lemma 2.2.** Starting at point  $(x_1, x_2, \dots, x_n, x_{n+1})$  in stage 0 of the SN, and traveling  $n$  edges on a primitive circuit, we arrive at point  $(x_{n+1}, x_1, x_2, \dots, x_n)$  in stage 0.

*Proof.* It follows immediately from the fact the network has  $n$  stages and along a single edge we travel from point  $(y_1, y_2, \dots, y_n, y_{n+1})$  to point  $(y_2, \dots, y_n, y_{n+1}, y_1)$  in the next stage. ■

Using Lemma 2.2, we observe that the number of primitive circuits in the  $n$ -stage all-bars SN is the same as the number of circuits,  $Z(n + 1)$ , in the pure cycling register of order  $n + 1$  [6], and, hence, we have the following result:

**Lemma 2.3.** The number of primitive circuits in the all-bars SN of order  $n$  is  $Z(n + 1) = 1/(n + 1) \sum_{d|n+1} \phi(d)2^{(n+1)/d}$ , where  $\phi(\cdot)$  is the Euler function [6].

The last important observation that helps to form an Eulerian circuit in the SN is formulated as the following:

**Lemma 2.4.** Two points on the same vertex differ only in their last bit.

We now describe a procedure for the construction of an Eulerian circuit in SN with a minimal number of crosses that by Lemmas 2.1 and 2.3 is  $Z(n + 1) - 1$ . At each step of the procedure, there is a *main circuit* that has resulted from the joining of primitive circuits in the previous steps. Initially, the main circuit is chosen to be the unique primitive circuit of weight zero. Next, the main circuit is extended by joining to it the (unique) circuit of weight one. At step  $i$ , the main circuit is extended by joining to it all the primitive circuits of weight  $i$  (in arbitrary order). This is always possible because the current main circuit contains all the points whose weight is less than  $i$  and, since each primitive circuit of weight  $i \geq 1$  has a point ending in a ONE, it can be joined (see Lemma 2.1 and Lemma 2.4) to the current main circuit. Therefore, all that is required is to choose, on each primitive circuit with weight greater than zero, a point ending with ONE. The vertices of these points are then cross-threaded. There are many different choices for these points and we describe one of them. Since the structure between any two consecutive stages is identical, we look only at points in stage  $r$  along the trellis, for some  $r$ ,  $0 \leq r \leq n - 1$ . In each primitive circuit, of weight greater than zero, we choose the point in stage  $r$  that is minimal in base-2, and, hence, ends in a ONE, among all the points of this circuit. The solution along this procedure results in all the cross-threading being in the same stage. This procedure is illustrated on the SN with 16 vertices per stage in Figure 1, where the vertices that are cross-threaded have crosses and the labeling of the points are written in each row. Note that in this one-dimension illustration stage 0 is duplicated.

This procedure can be extended to related networks. If instead of an SN, which is a circular  $n$ -stage shuffle exchange network (SEN), we take a circular  $k$ -stage SEN, of the same number of  $2^n$  vertices per stage, we do the following modifications: Let the definitions of weight and primitive circuits be the same as in the SN. Let  $d$  be the length of a primitive circuit in the circular 1-stage SEN. The integer  $d$  must be a divisor of  $n + 1$  since now the circuits are identical to the circuits of the pure cycling register of order  $n + 1$ .

**Lemma 2.5.** The number of primitive circuits in a circular  $k$ -stage SEN of order  $n$ , which include points that are cyclic shifts of  $(x_1, x_2, \dots, x_n, x_{n+1})$ , is  $g.c.d. (k, d)$ , where  $d$  is the length of the circuit which includes the point  $(x_1, x_2, \dots, x_n, x_{n+1})$  in the circular 1-stage SEN, and  $g.c.d.$  stands for the greatest common divisor.

*Proof.* Starting with the point  $(y_1, y_2, \dots, y_n, y_{n+1})$  [which is some cyclic shift of  $(x_1, x_2, \dots, x_n, x_{n+1})$ ] in stage 0, and traveling  $k$  edges, we arrive to point  $(y_{k+1}, \dots, y_{n+1}, y_1, \dots, y_k)$ , where subscripts are taken modulo  $n + 1$ , in the first stage. Since the length of the circuit in the circular 1-stage SEN is  $d$ ,

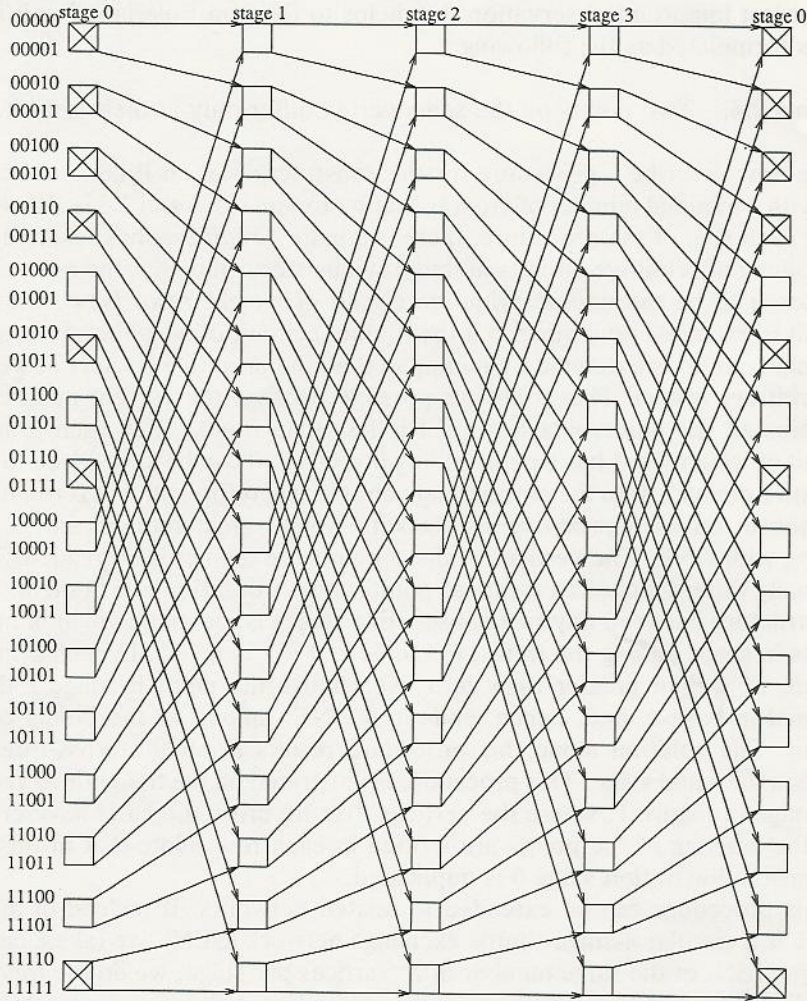


FIG. 1. A crossed SN with an Eulerian circuit.

$(y_1, y_2, \dots, y_n, y_{n+1}) = (y_{d+1}, \dots, y_{n+1}, y_1, \dots, y_d)$ . Therefore, after traveling *l.c.m.*  $(k, d)$  edges (where *l.c.m.* stands for the least common multiplier), we arrive back at point  $(y_1, y_2, \dots, y_n, y_{n+1})$  in the first stage for the first time. Since the length of the circuit in the circular 1-stage SEN is  $d$ , in  $k$  stages we have  $kd$  points with a representation that is a cyclic shift of  $(x_1, x_2, \dots, x_n, x_{n+1})$ . Thus, the number of primitive circuits in a  $k$ -stage SEN of order  $n$  that include points that are cyclic shifts of  $(x_1, x_2, \dots, x_n, x_{n+1})$ , is  $(dk)/[l.c.m. (k, d)] = g.c.d. (k, d)$ . ■

Now, note that in a circular  $k$ -stage SEN it is not necessarily that all primitive circuits have points ending with a ONE in stage  $r$ , for some  $r, 0 \leq r \leq k - 1$ . On

the other hand, any *g.c.d.*  $(k, d)$  points with the same labeling on *g.c.d.*  $(k, d)$  consecutive stages belong to *g.c.d.*  $(k, d)$  different primitive circuits. Moreover, any *g.c.d.*  $(k, d)$  points with the same labeling on stages  $a_1, a_2, \dots, a_t$ , with  $t = \text{g.c.d.}(k, d)$  and such that the sequence  $a_1, a_2, \dots, a_t$  includes all the residues modulo  $t$ , belong to *g.c.d.*  $(k, d)$  different primitive circuits. Since there are cycles of length  $n + 1$  in the circular 1-stage SEN, this shows that if  $k$  and  $n + 1$  are not relatively primes then it is necessary to put crosses in *g.c.d.*  $(k, n + 1)$  stages with indices covering all residues classes modulo *g.c.d.*  $(k, n + 1)$  in order to achieve an Euler circuit. As in the previous case, the cross-threading can be at vertices with points that are minimal in base-2 among all their shifts. For each minimal value like this we choose  $t = \text{g.c.d.}(k, d)$  stages  $a_1, a_2, \dots, a_t$ , such that the sequence  $a_1, a_2, \dots, a_t$  includes all the residues modulo  $t$ , and in these stages, the corresponding vertices are cross-threaded.

Other types of networks on which we can use our procedure are circular  $k$ -stage UMFA networks [5, 9]. The circular  $k$ -stage SEN is a special case of a circular  $k$ -stage UMFA network. Those networks are derived from unique path property (UPP) graphs [8]. A UPP graph is a directed graph with  $2^n$  vertices, each one with in-degree and out-degree two, and between any two vertices there is a unique path of length  $n$ . Given a UPP graph  $G$ , we construct the  $k$ -stage UMFA network  $N$  as follows: There is a directed edge between vertex  $i$  of stage  $r$ ,  $0 \leq r \leq k - 2$ , to vertex  $j$  of stage  $r + 1$  in  $N$  iff there is a directed edge from vertex  $i$  to vertex  $j$  of  $G$ . The  $k$ -stage SEN is derived from the well-known de Bruijn graph.

To see how the same procedure for finding Eulerian circuits on circular  $k$ -stage SEN works on circular  $k$ -stage UMFA, we will consider the following structure  $N^*$  derived from the circular  $k$ -stage UMFA network  $N$ .  $N^*$  has  $k$  stages, each one has  $2^{n+1}$  vertices labeled by all the binary  $(n + 1)$ -tuples. From vertex  $(x_1, x_2, \dots, x_n, x_{n+1})$  in stage  $r$ ,  $0 \leq r \leq k - 1$ , there is an edge to vertex  $(y_1, y_2, \dots, y_n, y_{n+1})$  in stage  $r + 1$  modulo  $k$  iff in  $N$  either from point  $(x_1, x_2, \dots, x_n, x_{n+1})$ , or from point  $(x_1, x_2, \dots, x_n, \bar{x}_{n+1})$ , there is an edge to point  $(y_1, y_2, \dots, y_n, y_{n+1})$ . One can easily derive the following:

**Lemma 2.6.**

- (i)  $N^*$  is a circular  $k$ -stage UMFA network with  $2^{n+1}$  vertices per stage.
- (ii) Let  $G$  and  $G^*$  be the corresponding UPP graphs for  $N$  and  $N^*$ . Then,  $G^*$  is the line graph of  $G$ .

A *factor* in a directed graph is a set of vertex disjoint directed circuits that includes all the vertices of the graph. As was proved by Mendelsohn [8], in each UPP graph with  $2^{n+1}$  vertices, there is a factor with  $Z(n + 1)$  circuits. There are  $f(m) = 1/m \sum_{d|m} \mu(d)2^{m/d}$  circuits of length  $m$ ,  $m | n + 1$ , in this factor, where  $\mu(\cdot)$  is the Mobius function [6], and we will call this factor the *base factor*. The primitive circuits in the circular 1-stage SEN is an example of a base factor. The joining of the circuits of this factor into a Hamiltonian circuit (de Bruijn sequence in the circular 1-stage SEN) gives the clue to the joining of

the corresponding primitive circuits in  $N$  into an Eulerian circuit. In  $G^*$ , we can find easily the Hamiltonian circuit. This is done by using the following *Buddy property* [2] of  $G^*$ . A directed graph has the Buddy property if, when two vertices have a common son, all their sons are identical. We cite the following lemma (see, e.g., [6]).

**Lemma 2.7.** Let  $C_1$  and  $C_2$  be two circuits in a graph  $G$  with the Buddy property. If there is an edge from a vertex on  $C_1$  to a vertex on  $C_2$ , then there is a circuit in  $G$  that contains all the vertices of  $C_1$  and  $C_2$ .

A simple proof is the following: Let  $v_1$  and  $u_1$  be two consecutive vertices on  $C_1$  ( $v_1 \rightarrow u_1$ ), and  $v_2$  and  $u_2$  two consecutive vertices on  $C_2$  ( $v_2 \rightarrow u_2$ ). Furthermore, there is a directed edge from  $v_1$  to  $u_2$ . Hence, by the Buddy property, there is an edge from  $v_2$  to  $u_1$ . Therefore, by taking the edges  $v_1 \rightarrow u_2$  and  $v_2 \rightarrow u_1$  (instead of  $v_1 \rightarrow u_1$  and  $v_2 \rightarrow u_2$ ) and all the other edges of  $C_1$  and  $C_2$ , we obtain a circuit  $C_3$  that contains all the vertices of  $C_1$  and  $C_2$ .

Using Lemma 2.7, we can form a Hamiltonian circuit in  $G^*$ . Initially, we take the base factor in  $G^*$ . Using Lemma 2.7, we can join two circuits together and apply this process until we join all the circuits into a Hamiltonian circuit. Now the procedure for generating an Eulerian circuit in  $N$  follows rather easily, but we cannot give the explicit construction in advance.

Finally, the same procedure that worked in the case of 2 points in a vertex works also in networks with  $m$  points in a vertex. Then, each stage has  $m^n$  vertices, each vertex has  $m$  points, and we say that vertex  $(x_1, x_2, \dots, x_n)$  is bar-threaded if the edge from point  $(x_1, x_2, \dots, x_n, x_{n+1})$ , where  $x_i \in \{0, 1, \dots, m-1\}$ , is to point  $(x_2, \dots, x_n, x_{n+1}, x_1)$ . This is an  $m$ -ary perfect shuffle. Again, a procedure similar to the one of constructing  $m$ -ary de Bruijn sequences [3] can be used.

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## REFERENCES

- [1] A. S. Acampora, M. J. Karol, and M. G. Hluchyj, Terabit lightwave networks: The multihop approach. *AT&T Tech. J.* **66** (1987) 21–35.
- [2] D. P. Agrawal, Graph theoretical analysis and design of multistage interconnection networks. *IEEE Trans. Comput.* **C-32** (1983) 637–648.
- [3] T. Etzion. An algorithm for constructing  $m$ -ary de Bruijn sequences. *J. Algorithms* **7** (1986) 331–340.
- [4] T. Etzion and A. Lempel, Algorithms for the generation of full-length shift-register sequences. *IEEE Trans. Info. Theory* **IT-30** (1984) 480–484.
- [5] D. Goldfeld and T. Etzion, UPP graphs and UMFA networks—Architecture for parallel systems, *IEEE Trans. on Comput.*, to appear.
- [6] S. W. Golomb, *Shift Register Sequences*. Aegean Park; Laguna Hills, CA (1982).
- [7] D. H. Lawrie, Access and alignment of data in array processor. *IEEE Trans. Comput.* **C-24** (1975) 1145–1155.

- [8] N. S. Mendelsohn, Directed graphs with unique path property. *Combinatorial Theory and Applications* (P. Erdos, A. Renyi, and V. T. Sos, Eds.). North-Holland, Amsterdam, London (1970) 783–799.
- [9] M. A. Sridhar and C. S. Raghavendra, Uniform minimal full-access networks. *J. Parallel Distributed Comput.* 5 (1988) 383–403.

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